UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/963,389	09/27/2001	Robert C. Hash	219.40445X00	9467

20457 7590 07/21/2003

ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-9889

EXAMINER
PATEL, PARESH H

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 07/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/963,389	HASH, ROBERT C.	
	Examiner	Art Unit	
	Paresh Patel	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 17-20* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

Claims 5 and 12 are objected to because of the following informalities:

Regarding claim 5, this claim should be depend from claim 4 because "the board tester" is not in claim 1. Appropriate correction is required.

Regarding claim 12, location of both signal pins (one with ground pin and another with power pin) inside a system is not clear. Also, pins are monitored but using what and how is not clear.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-11 and 17-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1, "connecting a first control signal to each first switching device", "connecting a second control signal to each second switching device" and "activating one of the first and second control signal", wherein connecting the control signals and then activation of these control signal is not clear because it is assumed that when signal is connected it means it is active. Hence, both signal are active in the beginning steps. Thus, later part i.e. activating one of the first and second control signal is not clear. Also, monitoring the signal pins using what is not clear.

Claims 2-11 and 20 are rejected because they depend from rejected claim.

Regarding claim 17, function or use of module pins are not clear. Also, monitors pins using what and how is not clear. Also claim language for "at least two switching devices" is not clear.

Claims 18-19 are rejected because they depend from rejected claim.

Examiner had made some changes, which are underline with italic font. These changes are made so Examiner can apply the art and can expedite the prosecution.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-15 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsui et al. (JP 57-204459).

Regarding claim 1, Matsui et al. (hereinafter Matsui) in fig. 1-2 discloses: A method for in-circuit socket test comprising: connecting a first switching device [emitter-collector of 8] to each signal pin [5] of a socket [7] and to a single ground pin [6] of the socket, connecting a second switching device [base-collector of 8] to each signal pin [5] of the socket [7] and to a single power pin [4] of the socket [7]; connecting a first control

signal [via 1 or 2] to each first switching device; connecting a second control signal [via 2 or 3] to each second switching device; activating one of the first control signal and the second control signal, the activation of the first control signal causing at least one of the signal pins to be connected to ground through the ground pin, activation of the second control signal causing at least one of the signal pins to be connected to power through the power pin [see fig. 2]; and monitoring the signal pins during the activating to detect open connections to each signal pin, ground pin and power pin [see Abstract].

Matsui in the abstract is silent about the socket being connected to a motherboard. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use motherboard, since it was known in the art that socket(s) is/are mounted on printed circuit board or motherboard in order to support the device (IC's) mounted on it and also to supply electrical signal(s) to that device from the motherboard.

Regarding claim 2, Matsui discloses only one transistor [8]. Matsui in the abstract do not teach or suggest the first switching device and the second switching device comprising Field-effect Transistors (FETs). It would have been obvious matter of design choice to use another transistor as the switching device, since applicant has not disclosed that use of another transistor solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with one transistor as disclosed by Matsui.

Regarding claim 3, Matsui discloses: the method according to claim 2, further comprising connecting the first control signal and the second control signal to a gate of the FETs [gate of 8's].

Regarding claim 4, Matsui discloses: the method according to claim 1, further comprising electrically connecting a board tester [10] to each signal pin, ground pin, and power pin of the socket, the monitoring [using 12 or 13] being performed by the board tester, the board tester performing the activation of the first control signal and the second control signal.

Regarding claim 5, Matsui discloses all the elements except: the method according to claim ~~1~~ 4 wherein the board tester comprises one of a HP3070 tester and a GENRAD tester. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use one of a HP3070 tester and a GENRAD tester, since it was known in the art that these tester are used for checking of bridging and shorts in the motherboard as further defined in background information of applicant's own disclosure.

Regarding claim 6, Matsui discloses: the method according to claim 1, further comprising inserting a module [8 of fig. 1 which includes transistor of fig. 2] into the socket [7], the first switching device and the second switching device residing on the module.

Regarding claim 7, Matsui discloses: the method according to claim 1, wherein a separate first control signal [via 1 or 2] is connected to each first switching device.

Regarding claim 8, Matsui discloses all the elements except: the method according to claim 1, wherein the same first control signal is connected to at least two first switching devices. It would have been obvious matter of design choice to use the same first control signal is connected to at least two first switching devices, since applicant has not disclosed that use of the same first control signal with two first switching devices solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with system as disclosed in fig. 1-2 by Matsui.

Regarding claim 9, Matsui discloses: the method according to claim 1, wherein a separate second control signal [via 2 or 3] is connected to each second switching device.

Regarding claim 10, Matsui discloses all the elements except: the method according to claim 1, wherein the same second control signal is connected to at least two second switching devices. It would have been obvious matter of design choice to use the same second control signal with two second switching devices, since applicant has not disclosed that use of the same second control signal with two second switching devices solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with one transistor as disclosed by Matsui.

Regarding claim 11, Matsui discloses all the elements except: the method according to claim 1, wherein the socket comprises one of a pinned grid array socket and a ball grid array socket. It would have been obvious matter of design choice to use one of a pinned grid array socket and a ball grid array socket, since applicant has not

disclosed that use of one of a pinned grid array socket and a ball grid array socket solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with system as disclosed by Matsui.

Regarding claim 12, Matsui in fig. 1-2 discloses: A system for in-circuit socket testing comprising: a module [8 of fig. 1], the module electrically attachable to a socket [7]; and a test fixture 10], the test fixture being electrically connected to all pins [1, 2, 3] of the socket through the printed circuit board, the test fixture supplying power [using 11] and ground [using 11] to power pins [1] and ground pins [3] of the socket, wherein open connections to pins of the socket are detected by monitoring the pins after at least one of connecting a signal pin to a ground pin through one at least two switching devices and connecting a signal pin to a power pin through another at least two switching devices [see abstract].

Matsui discloses all the elements except the module containing at least two switching devices, a printed circuit board, the printed circuit board containing a footprint for insertion of all pins of the socket. However, Matsui discloses one switching device [8 of fig. 2]. Matsui in the abstract is silent about the socket being connected to a printed circuit board and a footprint of printed circuit board for insertion of all pins of the socket. Matsui in the abstract do not teach or suggest the use of second switching device.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use printed circuit board with footprints, since it was known in the art that socket(s) is/are mounted on footprints of printed circuit board or motherboard in

order to support the device (IC's) mounted on it and also to supply electrical signal(s) to that device from the motherboard.

It would have been obvious matter of design choice to use another transistor as the second switching device, since applicant has not disclosed that use of another transistor solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with system of fig. 1-2 as disclosed by Matsui.

Regarding claim 13, Matsui discloses only one transistor [8]. Matsui in the abstract do not teach or suggest that two switching devices comprising Field-effect Transistors (FETs). It would have been obvious matter of design choice to use another transistor as the switching device, since applicant has not disclosed that use of another transistor solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with system of fig. 1-2 as disclosed by Matsui.

Regarding claim 14, Matsui discloses all the elements except: the system according to claim 12, wherein the socket comprises one of a pinned grid array and a ball grid array. It would have been obvious matter of design choice to use one of a pinned grid array socket and a ball grid array socket, since applicant has not disclosed that use of one of a pinned grid array socket and a ball grid array socket solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with system as disclosed by Matsui.

Regarding claim 15, Matsui discloses the system according to claim 12, wherein the printed circuit board includes test points test points on 10], the test fixture being

electrically connected to the pins of the socket through the test points on the printed circuit board.

Regarding claim 17, Matsui discloses: an in-circuit socket test module comprising: a plurality of module pins [4, 5, 6], the *module* pins being attachable to a socket [7], one module pin existing for each pin of the socket, each module pin being electrically isolated from each other on the module [8 of fig. 1]; and, wherein during an in-circuit socket test, power and ground are applied to the power pins and ground pins of the socket respectively, the pins of the socket being monitored to detect opens after at least one of the one at least two switching devices is controlled by the first control signal to connect a signal pin of the socket to a ground pin of the socket and the another at least two switching devices is controlled by the second control signal to connect the signal pin of the socket to a power pin of the socket.

However, Matsui discloses one switching device [8] and a first control signal [to gate of 8]. Masui does not teach or suggest in the abstract that at least two switching devices, one *of the* at least two switching devices being controllable by a first control signal to connect a signal pin of the socket to a ground pin of the socket, another *one of the* at least two switching devices being controllable by a second control signal to connect the signal pin to a power pin of the socket. It would have been obvious matter of design choice to use another transistor as the another switching device with the second control signal, since applicant has not disclosed that use of another switching device solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with system of fig. 1-2 as disclosed by Matsui.

Regarding claim 18, Matsui discloses only one transistor [8]. Matsui in the abstract do not teach or suggest that two switching devices comprise field-effect transistors (FETs). It would have been obvious matter of design choice to use another transistor as the switching device, since applicant has not disclosed that use of another transistor solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with system of fig. 1-2 as disclosed by Matsui.

Regarding claim 19, Matsui discloses only one switching device [8] with a control signal [to gate of 8]. Matsui does not teach or suggest in the abstract that the module according to claim 18, wherein the second control signal are connected to gates of the second field-effect transistor. It would have been obvious matter of design choice to use the second control signal with second switching devices such as second field effect transistor, since applicant has not disclosed that use of the second control signal with second switching devices solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with system as disclosed by Matsui.

Regarding claim 20, Matsui discloses all the elements except: the module according to claim ~~1~~ *17*, wherein the socket comprises one of a pinned grid array socket and a ball grid array socket. It would have been obvious matter of design choice to use one of a pinned grid array socket and a ball grid array socket, since applicant has not disclosed that use of one of a pinned grid array socket and a ball grid array socket solves any stated problem or is for any particular purpose and it appears that the invention would perform equally well with system as disclosed by Matsui.

Allowable Subject Matter

Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Prior art does not teach or suggest the test fixture controls a first control signal and a second control signal, the first control signal controlling the one at least two switching devices to connect a signal pin to a ground pin, the second control signal controlling the another at least two switching devices to connect the signal pin to a power pin as further define in the system according to claim 12.

Prior art to Rouchaud (US 5811977) does not teach or suggest the system including socket, tester, and module having two controllable switching devices and to detect open connections to each pin of the socket as further define in the claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 703-306-5859. The examiner can normally be reached on M-F (8:30 to 4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 703-308-1233. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Paresh Patel
June 12, 2003

VINH P. NGUYEN
PRIMARY EXAMINER
GROUP 2829
06/13/03